DOCKET NO: 211200US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

TOSHITADA SAITO : EXAMINER: TRIMMINGS, JOHN P.

SERIAL NO: 09/900,945 :

RCE FILED: MARCH 29, 2005 : GROUP ART UNIT: 2133

FOR: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDING PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS :

REQUEST FOR REFUND

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

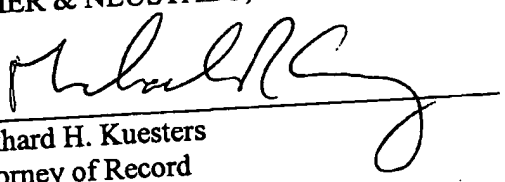
Applicant respectfully requests a refund of the $330.00 Extension for Response fee which corresponds to the second month extension in the above-identified application.

On October 29, 2004, the Patent and Trademark Office mailed a Final Office Action, and Applicant filed a response within 2 months on December 29, 2004. On March 21, 2005, the Patent and Trademark Office mailed an Advisory Action. Applicant's response to the Advisory Action was filed on March 29, 2005 with payment for a 2 month extension. However, since the three months shortened statutory period expired on March 21, 2005 (i.e., mailing date of the Advisory Action) only a one month extension was required. MPEP 706.07(f)(A). Copies of date-stamped filing receipts are enclosed to show the filing dates of Applicant's amendments.

Accordingly, Applicant respectfully requests a refund of the second month extension fee (i.e., $330.00 Extension for Response). Please credit the $330.00 overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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EHK:ZSS:dnf

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Dept.: E/M
By: EHK/ZSS/dnf

OSMM&N File No. 211200US2
Serial No. 09/900,945
In the matter of the Application of: Toshitada SAITO
For: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDING PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS

Due Date: January 29, 2005

The following has been received in the U.S. Patent Office on the date stamped hereon:

- Dep. Acct. Order Form
- Amendment Cover Letter
- Amendment (After Final)

COPY

Dept.: E/M

By: EHK/dnf

OSMM&N File No. 211200US2

Serial No. 09/900,945

In the matter of the Application of: Toshitada SAITO

For: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDIN
PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS

Due Date: March 29, 2005

The following has been received in the U.S. Patent Office on the date stamped hereon

- ■ Credit Card Form for $1,240.00
- ■ Dep. Acct. Order Form
- ■ Request for Extension of Time (2 months)
- ■ Request for Continued Examination (RCE)

DOCKET NO: 211200US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

TOSHITADA SAITO : EXAMINER: TRIMMINGS, J. P.

SERIAL NO: 09/900,945 :

FILED: JULY 10, 2001 : GROUP ART UNIT: 2133

FOR: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDING PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS :

AMENDMENT UNDER 37 C.F.R. § 1.116

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated October 29, 2004, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A system LSI being formed on one chip, comprising:

a storage circuit in which ~~at least one program has been~~ an operation program and a debug backup functional program are stored;

at least one processor circuit for carrying out a processing operation in accordance with said operation program, said processor circuit having a program counter, at least one computing unit and at least one register;

a peripheral circuit, capable of sending and receiving a signal to and from said processor circuit, for carrying out a predetermined logical operation in accordance with an input signal, said peripheral circuit having at least one functional block; ~~and~~

~~said system LSI further comprising~~

selection means for optionally selecting one output of said program counter, said computing unit and said register in said processor circuit, at least one output of said storage circuit, and one output of a plurality of internal signals in said peripheral circuit including an output of said functional block, and

selection control means for controlling selection of a result signal from any operation process in any place of said processor circuit, said storage circuit and said peripheral circuit, on the basis of a selection signal which is supplied from an outside of said system LSI via an external terminal; and

a debug backup circuit for carrying out a debug to a bug caused by said any operation process, on the basis of said debug backup functional program which is stored in said storage circuit.

Claim 2 (Currently Amended): A system LSI as set forth in claim 1, wherein said ~~processor circuit further comprises a~~ debug backup circuit ~~having~~ has an internal control signal generating portion for generating an internal control signal during a processing operation based on the debug backup functional program in the storage circuit, and said selection means carries out a selecting operation on the basis of said internal control signal, which is generated by said internal control signal generating portion of said processor circuit, and said selection signal which is supplied from the outside.

Claim 3 (Original): A system LSI as set forth in claim 1, wherein said selection means comprises:

a first selection circuit, provided in said processor circuit, for optionally selecting and outputting at least one value of said program counter, said computing unit, said register and said storage circuit;

a second selection circuit, provided in said peripheral circuit, for optionally selecting and outputting one of a plurality of internal signals in said peripheral circuit, which include the output of said functional block; and

a third selection circuit for optionally selecting one of the outputs of said first and second selection circuits to output the selected one to the outside.

Claim 4 (Original): A system LSI as set forth in claim 3, wherein said processor circuit further comprises a debug backup circuit having an internal control signal generating portion for generating an internal control signal during a processing operation, and said first through third selection circuits carry out a selecting operation on the basis of said internal control signal, which is generated by said internal control signal generating portion of said processor circuit, and said selection signal which is supplied from the outside.

Claim 5 (Currently Amended): A system LSI as set forth in claim 3, which further comprises a plurality of processor circuits, each of which is said processor circuit according to claim 3, and

wherein said second selection circuit carries out a selecting operation on the basis of a control signal which is generated while each of said plurality of processor circuits is operating, and

said third selection circuit optionally selects one of the output of said first selection means and the output of said second selection means on the basis of a control signal, which is generated while each of said plurality of processor circuits is operating, and a control signal which is supplied from the outside, to output the selected output to the outside.

Claim 6 (Original): A system LSI as set forth in claim 5, wherein each of said plurality of processor circuits comprises a debug backup circuit having an internal control signal generating portion for generating an internal control signal during a processing operation, and said first through third selection circuits carry out a selecting operation on the basis of said internal control signal, which is generated by said internal control signal generating portion of each of said plurality of processor circuits, and said selection signal which is supplied from the outside.

Claim 7 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a serial/parallel converter circuit for serial/parallel converting a selected signal to output the converted signal to the outside of said LSI.

Claim 8 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a parallel/serial converter circuit for parallel/serial converting a selected signal to output the converted signal to the outside of said LSI.

Claim 9 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a thinning-out circuit for thinning out selected signals at regular intervals to output the thinned-out signals to the outside of said LSI.

Claim 10 (Original): A system LSI as set forth in claim 1, wherein said LSI has a plurality of input/output terminals for sending and receiving signals to and from a system LSI peripheral device.

Claim 11 (Original): A system LSI as set forth in claim 10, wherein any one of said plurality of input/output terminals is used for inputting/outputting a monitor control signal for debug and a monitor signal.

Claim 12 (Original): A system LSI as set forth in claim 1, wherein said LSI further comprises an input terminal only for inputting a monitor control signal for debug, and an output terminal only for outputting the monitor signal after monitoring.

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application. Claims 1 and 2 are amended by the present amendment.

Claim amendments find support in the claims as originally filed and in the specification at least at page 9, line 33 to page 10, line 4. Thus, no new matter is added.

This amendment is submitted in accordance with 37 C.F.R. § 1.116, which after final rejection permits entering of amendments, canceling claims, complying with any requirement of form expressly set forth in a previous Office Action, or presenting rejected claims in better form for consideration on appeal. It is therefore respectfully requested that the present amendment be entered under 37 C.F.R. § 1.116.

In the outstanding Office Action, Claims 1-4 and 10-12 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,523,136 to Higashida in view of U.S. Patent No. 6,687,857 to Iwata et al. (herein "Iwata"); and Claims 5-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Higashida in view of Iwata and U.S. Patent No. 5,566,303 to Tashiro et al. (herein "Tashiro").

Initially, Applicant respectfully notes that the references in the Information Disclosure Statement filed October 28, 2004 were not indicated as having been considered by the Examiner. Accordingly, Applicant requests that a signed PTO Form-1449 be provided indicating consideration of those references.

Further, Applicant respectfully traverses the rejections of Claims 1-12 under 35 U.S.C. § 103(a) as unpatentable over Higashida in view of Iwata and Tashiro.

Amended Claim 1 is directed to a system LSI formed on one chip including a storage circuit storing an operation program and a debug backup functional program, processor

circuit with a program counter, and a peripheral circuit including a function block. In addition, the system LSI includes a selection means for optionally selecting one output of the program counter, the computing unit and the register in the processor circuit, at least one output of the storage circuit, and one output of a plurality of internal signals in the peripheral circuit including an output of the functional block. Further, the system LSI also includes a selection control means for controlling selection of a result signal from any operation process in any place of the processor circuit, the storage circuit and the peripheral circuit, based on a selection signal that is supplied from the outside of the system LSI via an external terminal. The system LSI also includes a debug backup circuit for carrying out a debug to a bug caused by any operation process, on the basis of the debug backup functional program that is stored in the storage circuit.

Applicant respectfully submits that Higashida does not teach or suggest a system LSI on one chip including a debug backup circuit for carrying out a debug. As noted in the outstanding Office Action, Higashida describes peripheral circuits in FIG. 1.[1] However, Higashida describes only peripheral circuits 20 and 30 in FIG 1. Further, Higashida describes that an internal bus is further connected to peripheral circuits such as a bus arbiter, which are not shown in the figure for simplicity reason.[2] Thus, although Higashida indicates peripheral circuits in an LSI chip from this description, Higashida indicates that internal signals are outputted from the peripheral circuits to an outside of the LSI as an object of the debug. Hence, it appears that Higashida does not have internal peripheral circuits as an object of debugging, and thus does not appear to teach or suggest "[a] system LSI formed on one chip, comprising . . . a peripheral circuit [and] selection means for optionally selecting . . . one output of a plurality of internal signals in said peripheral circuit," as recited in Claim 1.

[1] Office Action at page 3, lines 1-2.
[2] Higashida at column 1, lines 52-55.

Further, Applicant respectfully submits that Higashida does not teach or suggest the claimed selection means, and further Applicant traverses the assertion in the outstanding Office Action that Higashida discloses selection means at column l, lines 22-37, at column 7, lines 15-30, and in FIGS. 2 and 3.[3] The cited column 1 passage does not describe a selection means. The cited column 7 passage of Higashida indicates that an instruction execution processing portion 2c transmits a control signal via a CPU internal bus 2d. However, Applicant submits that Higashida does not disclose the selection means and a selection control means in that cited passage. Further, Higashida, shows a detailed configuration of a CPU core in FIG. 2 and a detailed configuration of a multiplexer 8 in FIG. 3. However, Higashida indicates that the multiplexer 8 selects any of signals from the internal bus corresponding to test mode instruction signal TPl and TP2 that are externally supplied via signal input terminal 9, which is different than the claimed approach in which selection control means 4, internally provided in the LSI, controls the selection means 30.

Further, Applicant respectfully traverses the assertion in the Office Action that Higashida performs "a selector control by way of a signal via an external terminal."[4] Higashida does not disclose a selection control means that outputs the selection control signal to the selection means responsive to the external selection signal. As indicated in FIG. 1, the device of Higashida merely includes a DSU-adapted debug device 20 that is externally provided and controls DSU 2a via pin terminal 10 of the LSI. Furthermore, Higashida indicates that the detailed control for the internal bus is performed by reading the program through the terminal 22 of the DSU-adapted debug device 20 from the internal bus signal display software (SF) 30a provided in the computer 30. On the contrary, a one-chip system LSI according to the present invention comprises a storage circuit including a debug backup program for internally controlling debugging in the LSI. Thus, Higashida does not teach or

[3] Office Action at page 3, lines 3-5.
[4] Office Action at page 3, line 5.

suggest "[a] system LSI being formed on one chip, comprising . . . a storage circuit in which an operation program and a debug backup functional program are stored," as recited in amended Claim 1.

Further, Applicant respectfully submits that Iwata and Tashiro also do not disclose the claimed features. Thus, the combined teachings of Higashida, Iwata and Tashiro do not teach or suggest the features of the independent claims. Accordingly, Applicant respectfully submits that independent Claim 1 and claims depending therefrom are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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P.C.

ATTORNEYS AT LAW

Docket No.: 211200US2

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 09/900,945
Applicants: Toshitada SAITO
RCE Filing Date: March 29, 2005
For: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDING PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS
Group Art Unit: 2133
Examiner: TRIMMINGS, J. P.

SIR:

Attached hereto for filing are the following papers:

REQUEST FOR REFUND (Duplicate)
DATE-STAMPED FILING RECEIPT DATED DECEMBER 29, 2004
DATE-STAMPED FILING RECEIPT DATED MARCH 29, 2005
AMENDMENT (COPY)

Our check in the amount of **$0.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Docket No. 211200US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Toshitada SAITO

SERIAL NO: 09/900,945 GAU: 2133

RCE FILED: Herewith EXAMINER: TRIMMINGS, J. P.

FOR: ONE-CHIP SYSTEM LARGE-SCALE INTEGRATED CIRCUIT INCLUDING PROCESSOR CIRCUIT AND ITS PERIPHERAL CIRCUITS

REQUEST FOR EXTENSION OF TIME UNDER 37 C.F.R. 1.136

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

It is hereby requested that a two month extension of time be granted to March 29, 2005 for

- ☐ filing a response to the Official Action dated:
- ☐ responding to the requirements in the Notice of Allowability dated:
- ☐ filing the Formal Drawings. The Issue Fee due has been timely filed.
- ☐ responding to the Notice to File Missing Parts of Application dated:
- ■ filing a Request for Continued Examination (RCE). A timely response to the final rejection, due January 29, 2005 was filed on December 29, 2004.
- ☐ filing an Appeal Brief. A Notice of Appeal was filed on:
- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown below is reduced by one-half.

The required fee of $450.00 is enclosed herewith by credit card payment and any further charges may be made against the Attorney of Record's Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Adjustment date: 07/20/2005 SDIRETA1
03/30/2005 CCHAU1 00000030 09900945
01 FC:1252 -450.00 OP

07/20/2005 SDIRETA1 00000004 09900945
01 FC:1251 120.00 OP

Respectfully Submitted,

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03/30/2005 CCHAU1 00000030 09900945
01 FC:1252 450.00 OP

Refund Ref: 0030023622 $330.00
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